QNX BSP for phyFLEX-i.MX6

FULL Version
with Graphics Support
by IBV - Echtzeit- und Embedded GmbH & Co. KG

Subject:	Release Notes
Version:	1.1, QNX 6.5.0SP1
Date:	21.02.2014

1. Features

1.1. Components of the BASE Version of the BSP

Component	Format	Features, Notes
Startup (BASE version)	Source	♦ Reads out MAC address from eFUSE ♦ Configurable DDR3 RAM size ♦ Supports QNX SMP
Serial	Source	♦ QNX character device driver (devc-) ♦ Supports i.MX6 UART4 (phyFLEX signals X_UART_0) ♦ Supports i.MX6 UART3 (phyFLEX signals X_UART_1) ♦ RTS/CTS handshake supported on UART4 ♦ Driver is interrupt driven (no DMA support)
FEC Network	Source	♦ QNX network driver DLL for io-pkt network stack (devnp-) ♦ Supports i.MX6 Gigabit Ethernet Controller ♦ 10/100 MBit speed ♦ Half / full duplex mode ♦ MAC address is used from configuration in eFUSE

1.2. Components of the FULL Version of the BSP

Component	Format	Features, Notes
Startup (FULL version)	Source	♦ Reads out MAC address from eFUSE ♦ Configurable DDR3 RAM size ♦ Supports QNX SMP
SPINOR	Source	♦ QNX flash file system driver (flash-) ♦ Supports SPI NOR flash (N25Q128A) on phyFLEX-i.MX6
SD	Source	♦ QNX file system driver (devb-) based on QNX MMC driver framework ♦ Supports i.MX6 uSDHC3 Controller (phyFLEX signals X_SD0) ♦ Supports i.MX6 uSDHC2 Controller (phyFLEX signals X_SD1) ♦ Driver is interrupt driven (no DMA support)
SATA	Binary	♦ QNX file system driver (devb-) ♦ Supports i.MX6 SATA Controller (phyFLEX signals (X_SATA0) Driver is shipped as original binary as provided by the operating system vendor in the original i.MX6 reference BSP and without support.

I2C	Source	♦ QNX I2C master driver (i2c-) ♦ Supports i.MX6 I2C1 Controller in master mode (phyFLEX on board) ♦ Supports i.MX6 I2C2 Controller in master mode (phyFLEX signals on X_I2C0_SDA, _SCL) ♦ Supports i.MX6 I2C3 Controller in master mode (phyFLEX signals on X_I2C1_SDA, _SCL)
USB	Binary	♦ QNX USB driver DLL for io-usb USB stack (devu-) ♦ Supports i.MX6 USB Host1 Controller (EHCI) with USB PHY2 in high speed mode (phyFLEX signals X_USB1) _Driver is shipped as original binary as provided by the operating system vendor in the original i.MX6 reference BSP and without support._
SPI	Source	♦ QNX SPI master driver based on QNX SPI Framework ♦ Supports i.MX6 ECSPI3 Controller in master mode (phyFLEX signals X_SPI0_...) ECSPI3 can not be used when SPI NOR driver is running. ♦ Supports i.MX6 ECSPI5 Controller in master mode (phyFLEX signals X_SPI1_...) ♦ QNX SPI master API library as binary without support ♦ Supports transfers with 1...32bit in normal mode and 8 / 16 / 32bit transfers in burst mode ♦ Supports control of up to 4 slave select signals per controller ♦ The driver is interrupt driven, DMA based transfers are not supported.
PCIe	Source	♦ QNX PCI driver (pci-) ♦ Supports i.MX6 PCIe bus (phyFLEX signals X_PCIE0) ♦ Message Signaled Interrupts (MSI) are not supported by QNX
CAN	Source	♦ QNX CAN driver based on QNX CAN Framework ♦ Supports i.MX6 FLEXCAN Controller (phyFLEX signals X_CAN0_RXD, X_CAN0_TXD) ♦ Supported baud rates: 20K, 25K, 50K, 100K, 125K, 250K, 500K, 1M ♦ Extension for transmission of CAN frames with payload sizes other than eight and remote frames ♦ Ready for use with EMBRICS ioCAN

1.3. Optional Driver Modules (not part of FULL Version of the BSP)

GPIO		on request
TOUCH		on request
AUDIO		on request
GRAPHICS	Source	◆ QNX graphics driver DLL for io-display (devg-) ◆ Supports i.MX6 graphic controller for applications working with the QNX GF interface and QNX Photon ◆ Supported display interface: LVDS ◆ Configurable bit mapping (SPWG/JEIDA) for LVDS display ◆ Configurable display colour depth (18/24 bpp) ◆ Frame buffer access (no hardware acceleration) ◆ Configurable display resolution (supported pixel clock 6...85 MHz) ◆ Supported pixel formats: ARGB8888, RGB888, RGB565 Limitations: ◆ Only one IPU (IPU1) is supported ◆ Only one display interface (DI0) is supported ◆ Only one LVDS channel (LVDS0) is supported ◆ Only one graphics layer is supported ◆ There is no support for alpha-blending or chroma-keying

1.4. Further BSPs for PHYTEC Boards

A complete list of all available QNX Board Support Packages for embedded boards by PHYTEC Messtechnik GmbH is available at:
http://www.ibv-augsburg.net/media/pdf/QNX_BSP_Overview_PHYTEC.pdf

2. General Information

2.1. Features of the BSP

The features of this Board Support Package and the Application Programming Interface (API) are defined and limited by the underlying QNX reference BSPs. Changes in the target system and/or peripheral components may require an adaption of the BSP. Therefore the BSP is provided in source code.

2.2. Dynamic voltage and Frequency Scaling (DVFS)

When running QNX, the CPU is clocked with the frequency selected by the boot loader "barebox".

Dynamic voltage and frequency scaling (DVFS) is not supported in QNX!

Important note:
Additional measures for cooling are necessary. Without additional measures, the board may be damaged. Please discuss this issue with your board vendor.

3. Target System

- Phytec CPU Module phyFLEX-i.MX6 (PCB#1362.1):
  - Freescale i.MX6 applications processor Quad, revision TO1.2
  - 1 GB DDR3 RAM (size configurable)
  - Tested and released for 800 MHz clock
- Phytec Baseboard phyFLEX Carrier Board PBA-B-01 (PCB#1364.3)
- Tested PCIe card: INTEL PRO/1000 Gigabit Ethernet Adapter
- Tested display: PHYTEC LCD-018-070-KAP (for optional driver module "devg")
- Operating system QNX 6.5.0 with SP1
- Boot loader barebox 2012.02.0 (Apr 23 2013 - 17:08:22)

4. Host Development System

- QNX Software Development Platform 6.5.0SP1
- Terminal emulation program (Qtalk, Momentics IDE Terminal, tip, HyperTerminal, etc.)
- RS-232 serial port or a USB-to-serial adapter, and a straight-through serial cable
- Ethernet link

5. Known Issues for this BSP

- Ethernet driver: The maximum supported speed is 100MBit. See also i.MX6 Errata ERR004512, "ENET system limitation". As workaround there is an option in the Ethernet driver to limit auto negotiation speed to 100MBit.
- SD card driver supports only one host controller and one card at a time. To support both SD card slots on the phyFLEX board, the driver must be started in two instances.
- The PCIe driver uses the same PLL as the SATA controller, and resets it during PCIe initialization. Therefore, the PCIe driver must be started before the SATA driver.
- PCI driver: It is necessary to reset a PCI card when the PCI driver is started. The PCI driver supports the configuration of a GPIO for resetting the PCI card. The phyFLEX carrier board does not support resetting the PCI card via a GPIO. The RESET button must be pressed manually (after power up) before the PCI driver is started. This issue must be considered in the design of a custom base board.
- The PCIe driver supports one PCIe lane with one PCIe device. If an external bridge is placed on the custom hardware, an adaption of the driver may be necessary.

6. Change History

6.1. Revision 1.1

♦ CAN driver added to FULL Version, BASE Version is unchanged
  ♦ Supports transmission of CAN frames with payload sizes other than eight
  ♦ Support of remote frames
  ♦ API distinguishes 11bit (CAN 2.0A) and 29bit (CAN 2.0B) identifiers
  ♦ Byte order within the frames during send and receive is not changed

6.2. Revision 1.0

♦ Adapted for phyFLEX-i.MX6 Board
♦ Support of NOR SPI flash on phyFLEX board
♦ Startup: configuration for SDRAM size added
♦ Bugfixes applied on i.MX6 QNX6 Reference BSP:
  ♦ Serial driver: correct handling of line status
  ♦ Network driver: Support auto negotiation with speed limit to 100 MBit/s
  ♦ Network driver: Workaround for i.MX6 errata
    ERR006358 "ENET: Write to Transmit Descriptor Active Register (ENET_TDAR) is ignored"
  ♦ SPI driver: support of different SPI transfer lengths and SPI message sizes
  ♦ SPI driver: support of clock polarity and clock phase
  ♦ SPI driver: support of SPI clock setting

7. Sales / Technical Support

To get this BSP or to obtain technical support for the BSP, please contact:

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