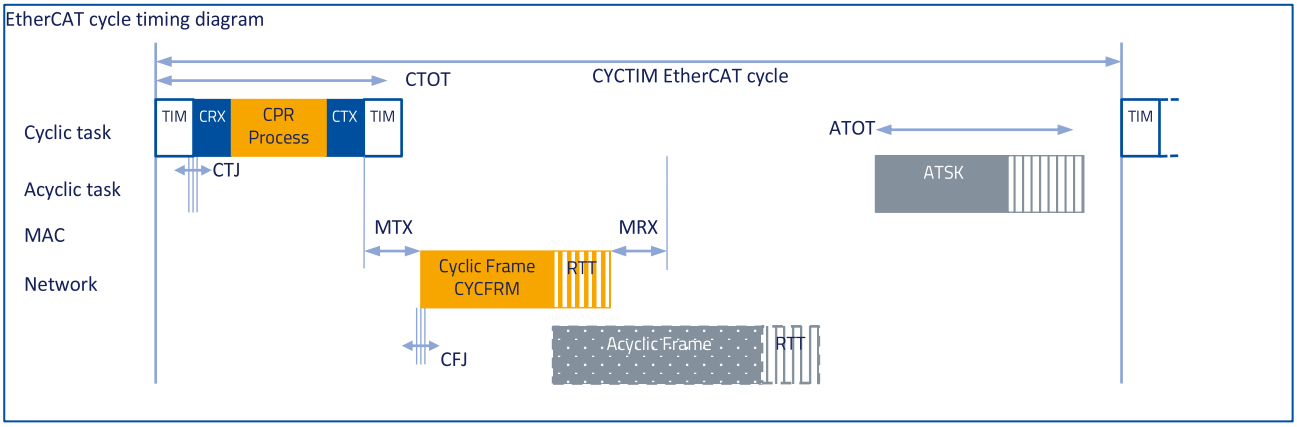
icECAT. EtherCAT Master Stack

Benchmark

Target System: TI AM64x / AM243x, R5F FreeRTOS

- CPU: Texas Instruments AM64x @800 MHz, ARM Cortex-R5F
- Board: Texas Instruments TMDS64EVM
- MAC: PRU_ICSSG1 (TI Dual-MAC firmware)
- Operating system: FreeRTOS v10.4.3, TI MCU+ SDK AM64x
- Optimizations: Execution from TCM, MSRAM
- EtherCAT software: icECAT EtherCAT Master Stack, v1.9
  icNET Optimized Link Layer Driver for TI ENET, v2.3
- Synchronization: Distributed Clocks, master mode
- EtherCAT network: 23 EtherCAT slaves (4x Ethernet 100BaseTX, 19x E-Bus)
- EtherCAT cyclic frame: PDUs: 2x DC + MBX IRQ + Process Data (LRW + LWR + LRD) + BRD => Σ 156 bytes
- EtherCAT acyclic frame: Chained to one cyclic task
- Test application: ecatm-sample-appl, performance monitor

EtherCAT cycle timing diagram



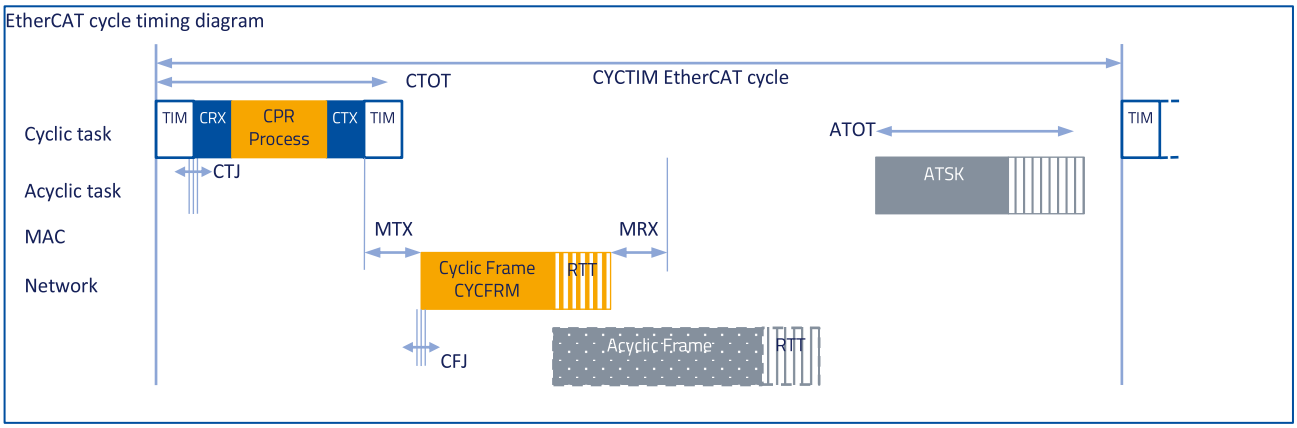
				AM64x R5F
Cyclic Task				
Receive last cyclic frame (by icECAT Master)	CRX	µs	ave.	12
Process cyclic data (simulated by application) (100x read access, 100x write access to process image)	CPR	µs	ave.	4
Send next cyclic and acyclic frame (by icECAT Master)	CTX	µs	ave.	12
Cyclic task overall, incl. processing, management of cycle timer	CTOT	µs	ave.	30
Acyclic Task				
Acyclic task (continuous CoE communication with one slave)	ATOT	µs	ave.	47
Network				
Cyclic frame time on the network (180 bytes)	CYCFRM	µs	calc.	14.4
Network round trip time (23 slaves)	RTT	µs	calc.	12.2
Jitter (with cyclic and acyclic load)				
Cyclic timer jitter (interrupt latency, thread scheduling of operating system)	CTJ	µs	min. max.	+2 +18
Cyclic frame jitter measured at DC reference slave incl. DC timer adjustment in master, const. processing time	CFJ	µs	min. max.	-11 +22
Cycle time used (23 slaves, cyclic frame with 156 bytes)	CYCTIM			100 µs

icECAT. EtherCAT Master Stack

Benchmark

Target System: TI AM69, Linux

- CPU: Texas Instruments AM69 8x ARM Cortex-A72 @2000 MHz
- Board: Texas Instruments SK-AM69
- MAC: MCU CPSW2G
- Operating system: Linux j784s4-evm 6.1.46-rt13-g833521d9b3 #1 SMP PREEMPT_RT Wed Dec 6 17:55:24 UTC 2023 aarch64 aarch64 aarch64 GNU/Linux
- Optimizations: Core isolation, set affinity mask of irq and kernel threads, set priority of rx/tx Ethernet interrupts
- EtherCAT software: icECAT EtherCAT Master Stack, v1.9
  icNET Standard Link Layer Driver for Linux, v1.2
- Synchronization: Distributed Clocks, master mode
- EtherCAT network: 23 EtherCAT slaves (4x Ethernet 100BaseTX, 19x E-Bus)
- EtherCAT cyclic frame: PDUs: 2x DC + MBX IRQ + Process Data (LRW + LWR + LRD) + BRD => Σ 156 bytes
- EtherCAT acyclic frame: Chained to one cyclic task
- Test application: ecatm-sample-appl, performance monitor



				AM69 Linux STD
Cyclic Task				
Receive last cyclic frame (by icECAT Master)	CRX	µs	ave.	4.3
Process cyclic data (simulated by application) (100x read access, 100x write access to process image)	CPR	µs	ave.	0.9
Send next cyclic and acyclic frame (by icECAT Master)	CTX	µs	ave.	6.4
Cyclic task overall, incl. processing, management of cycle timer	CTOT	µs	ave.	11.6
Acyclic Task				
Acyclic task (continuous CoE communication with one slave)	ATOT	µs	ave.	4.7
Network				
Cyclic frame time on the network (180 bytes)	CYCFRM	µs	calc.	14.4
Network round trip time (23 slaves)	RTT	µs	calc.	12.2
Jitter (with cyclic and acyclic load)				
Cyclic timer jitter (interrupt latency, thread scheduling of operating system)	CTJ	µs	min. max.	+2.6 +24.2
Cyclic frame jitter measured at DC reference slave incl. DC timer adjustment in master, const. processing time	CFJ	µs	min. max.	-12.0 +34.8
Cycle time used (23 slaves, cyclic frame with 156 bytes)	CYCTIM			200 µs
CPU load measured with “htop” (for the core running icECAT Master, incl. kernel threads)		%		27.3

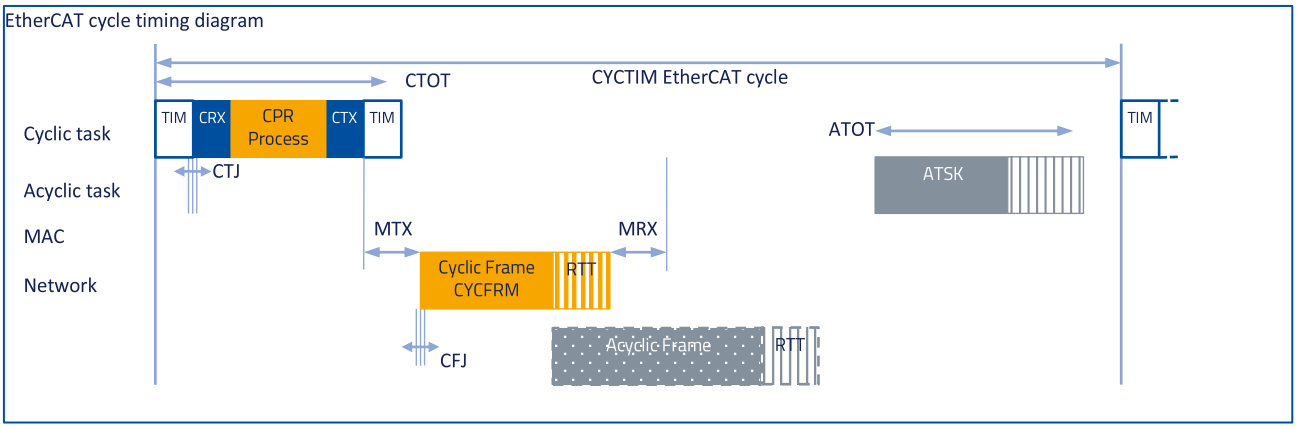
icECAT. EtherCAT Master Stack

Benchmark

Target System: NXP i.MX 8M Plus, Linux

- CPU: NXP i.MX 8M Plus, 4x ARM Cortex-A53 @ 1.6 GHz
- Board: PHYTEC phyBOARD-Pollux i.MX 8M Plus
- MAC: Internal FEC Ethernet MAC
- Operating system: Linux phyboard-pollux-imx8mp-3 5.4.70-rt40-bsp-yocto-fsl-i.mx8mp-pd21.1.2 #1 SMPPREEMPT_RT Tue May 31 11:42:46 UTC 2022 aarch64 GNU/Linux
- Optimizations: Core isolation, set affinity mask of irq and kernel threads, set priority of rx/tx Ethernet interrupts
- EtherCAT software: icECAT EtherCAT Master Stack, v1.9
  icNET Optimized Link Layer Driver for NXP FEC, v2.0.1 [OPT]
  icNET Standard Link Layer Driver for Linux, v1.2 [STD]
- Synchronization: Distributed Clocks, master mode
- EtherCAT network: 23 EtherCAT slaves (4x Ethernet 100BaseTX, 19x E-Bus)
- EtherCAT cyclic frame: PDUs: 2x DC + MBX IRQ + Process Data (LRW + LWR + LRD) + BRD => Σ 156 bytes
- EtherCAT acyclic frame: Chained to one cyclic task
- Test application: ecatm-sample-appl, performance monitor

EtherCAT cycle timing diagram



				i.MX8 MP [OPT]	i.MX8 MP [STD]
Cyclic Task					
Receive last cyclic frame (by icECAT Master)	CRX	µs	ave.	8.2	7.1
Process cyclic data (simulated by application) (100x read access, 100x write access to process image)	CPR	µs	ave.	12.0	1.7
Send next cyclic and acyclic frame (by icECAT Master)	CTX	µs	ave.	1.4	11.1
Cyclic task overall, incl. processing, management of cycle timer	CTOT	µs	ave.	21.6	19.9
Acyclic Task					
Acyclic task (continuous CoE communication with one slave)	ATOT	µs	ave.	18.0	5.0
Network					
Cyclic frame time on the network (180 bytes)	CYCFRM	µs	calc.	14.4	14.4
Network round trip time (23 slaves)	RTT	µs	calc.	12.2	12.2
Jitter (with cyclic and acyclic load)					
Cyclic timer jitter (interrupt latency, thread scheduling of operating system)	CTJ	µs	min. max.	+4.3 +32.6	+4.6 +55.0
Cyclic frame jitter measured at DC reference slave incl. DC timer adjustment in master, const. processing time	CFJ	µs	min. max.	-54.8 +57.2	-47.7 +123.2
Cycle time used (23 slaves, cyclic frame with 156 bytes)	CYCTIM			125 µs	500 µs
CPU load measured with “htop” (for the core running icECAT Master, incl. kernel threads)		%		48.5	13.4

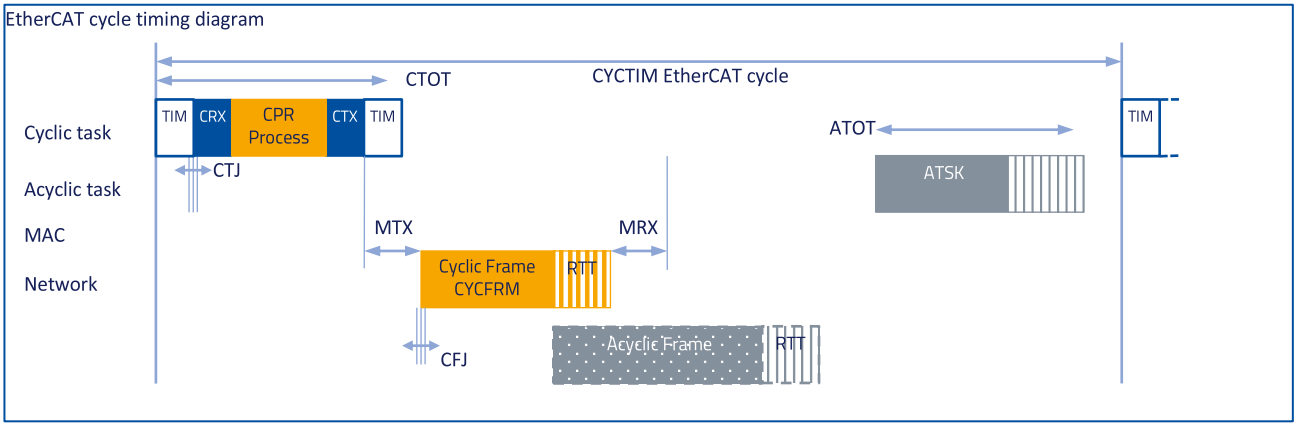
icECAT. EtherCAT Master Stack

Benchmark

Target System: Intel Celeron 3955U, Linux

- CPU: Intel(R) Celeron(R) CPU 3955U, 2 cores @ 2.00GHz
- Board: JETWAY NF731-3955U
- MAC: Intel I211
- Operating system: Linux 5.10.0-9-rt-amd64 #1 SMP PREEMPT_RT Debian 5.10.70-1 (2021-09-30) x86_64 GNU/Linux
- Optimizations: Core isolation
- EtherCAT software: icECAT EtherCAT Master Stack, v1.9
  icNET Opt. Link Layer Driver for Intel 210/211, v2.5.1 [OPT]
  icNET Opt. Link Layer Driver for Intel 210/211, with time-triggered send [OPT-TTS]
  Synchronization: Distributed Clocks, master mode
- EtherCAT network: 23 EtherCAT slaves (4x Ethernet 100BaseTX, 19x E-Bus)
- EtherCAT cyclic frame: PDUs: 2x DC + MBX IRQ + Process Data (LRW + LWR + LRD) + BRD => Σ 156 bytes
- EtherCAT acyclic frame: Chained to one cyclic task
- Test application: ecatm-sample-appl, performance monitor

EtherCAT cycle timing diagram



				[OPT]	[OPT-TTS]
Cyclic Task					
Receive last cyclic frame (by icECAT Master)	CRX	µs	ave.	1.6	1.7
Process cyclic data (simulated by application) (100x read access, 100x write access to process image)	CPR	µs	ave.	1.1	1.1
Send next cyclic and acyclic frame (by icECAT Master)	CTX	µs	ave.	1.2	7.8
Cyclic task overall, incl. processing, management of cycle timer	CTOT	µs	ave.	3.9	10.6
Acyclic Task					
Acyclic task (continuous CoE communication with one slave)	ATOT	µs	ave.	2.4	2.3
Network					
Cyclic frame time on the network (180 bytes)	CYCFRM	µs	calc.	14.4	14.4
Network round trip time (23 slaves)	RTT	µs	calc.	12.2	12.2
Jitter (with cyclic and acyclic load)					
Cyclic timer jitter (interrupt latency, thread scheduling of operating system)	CTJ	µs	min. max.	+2.5 +18.5	+2.5 +19.2
Cyclic frame jitter measured at DC reference slave incl. DC timer adjustment in master, const. processing time	CFJ	µs	min. max.	-10.1 +23.8	-0.3 +0.3
Cycle time used (23 slaves, cyclic frame with 156 bytes)	CYCTIM			100 µs	100 µs
CPU load measured with “htop” (for the core running icECAT Master)		%		14.9	28.2